HITACHI AND RENESAS TECHNOLOGY JOINTLY RELEASE THE DEVELOPMENT OF MEMORY CELL TECHNOLOGY FOR 4-GIGABIT AG-AND FLASH MEMORY

- Offering world's smallest cell area and fastest programming speed -

Tokyo, December 11, 2003 --- Hitachi, Ltd. (TSE:6501, NYSE:HIT) and Renesas Technology Corp. today announced the development of a basic flash memory cell technology that achieves the world's smallest cell area of 0.016 μm^2 (on a 1-bit basis) and fastest programming speed of 10 Mbytes/sec. This basic memory cell technology improves the source-drain structure of an AG-AND (Assist Gate-AND) *[1] flash memory cell featuring multi level cell technology*[2] and high speed, enabling the memory cell area to be reduced by approximately 30% when using a 90 nm process.

Renesas Technology plans commercial production of 4-Gigabit(Gbit) AG-AND flash memory based on this technology in the third quarter of 2004, and will offer compact, high-density, high-speed recording media for the "ubiquitous computing society."

High-density flash memory is beginning to permeate our lives as a bridge medium (information delivery device), especially in mobile applications, including use as image storage memory for digital cameras and mobile phones, and USB storage as replacements for floppy disk drives. Next-generation flash memory cards offering portability of large-volume, high-quality moving picture data such as movies will require significantly high density and higher programming speeds to handle fast data downloads.

In response to these needs, in 2001 Hitachi and Renesas Technology jointly developed a first-generation AG-AND flash memory offering a high programming speed of 10 Mbytes/sec through the use of assist gates (AGs) to prevent inter-cell interference together with multilevel cell technology, and Renesas Technology currently mass-produces 130 nm process 1-Gbit AG-AND flash memory. However, to meet the need for high density while maintaining high speed operation, it became necessary to make advances in memory cell structure to restrict lateral expansion by altering the source-drain structure*[3], and minimize the memory cell area as far as physical limitations allow.

Against this backdrop, Hitachi's Central Research Laboratory and Renesas Technology collaborated in the development of a basic technology for second-generation AG-AND flash memory that offers both high-speed writing and a fine process. The features of this newly developed technology are summarized below.

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(1) New memory cell structure providing high density

The source and drain of a memory cell transistor are formed as an inversion layer*[4] that appears in the silicon substrate when a voltage is applied to the AG, instead of the conventional diffusion layer. As the inversion layer is formed only in the extremely shallow region of the substrate just beneath the AG, there is no lateral spread. As a result, it has become possible to reduce the memory cell area from the previous 6 F^2 (F: feature size) to the physical limit of 4 F^2. Through combination with multilevel cell technology, the area per bit has become 2 F^2, and the world's smallest memory cell has been achieved, at 0.016 μm^2 for a 4-gigabit device using a 90 nm process. This represents an approximately 30% decrease compared with previous 130 nm process first-generation memory cells, enabling high-density flash memory cards to be realized.

(2) High-speed writing

High-speed memory cell programming at a low voltage have been made possible by the hot electron injection method*[5] used with the 1-Gbit product. In developing the 4-Gbit product, a maximum programming speed of 10 Mbits/sec has been achieved even with the use of multilevel technology.

This new technology makes possible fast downloading and portability of large-volume content data such as moving pictures and music. As a result, usage scenarios previously restricted to digital cameras and PCs can now be extended to mobile terminals and digital home appliances, expanding the range of system solutions that employ flash memory as a storage medium.

These results was announced at the 2003 IEEE International Electron Devices Meeting (IEDM) being held in Washington, D.C. from December 7, 2003.

[Notes]

(1) AG-AND (Assist Gate-AND) is a flash memory cell jointly developed by Hitachi and Renesas Technology. The cell structure employs original Hitachi and Renesas Technology field isolation technology comprising a combination of alternating assist gates that prevent inter-cell interference, enabling a smaller cell area and high-speed programming.

(2) Multi level cell technology: A technology suitable for high-density flash memory, effective in reducing chip size, whereby four or more values, such as 00, 01, 10, and 11, can be held as opposed to the usual two values, 0 and 1, of ordinary memory. When four values are used, one cell does the work of two ordinary cells.

(3) lateral expansion by altering the source-drain structure : In the first generation, a source and drain are formed by means of a diffusion layer* using the ion implantation method in the same way as ordinary MOS (Metal-Oxide-Semiconductor) transistors, but as this diffusion layer extends laterally, it is an obstacle to achieving finer memory cells.

*Diffusion layer: Ions are implanted into a silicon substrate, and high-density electrons are generated by applying a voltage to this region. This is the usual method for forming the source and drain of an MOS transistor.

(4) Inversion layer: A high-density electron region generated in the extremely shallow region of a silicon substrate when a voltage is applied to the gate. Used as an MOS transistor channel.

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(5) Hot electron injection method: A programming method whereby high-energy “hot” electrons accelerated by a channel field are injected into a floating gate. The cell programming time is 10 μs or less, an order of magnitude faster than with the conventional tunnel programming method.

[References]

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