Hitachi and Renesas Technology Develop Phase-Change Memory Cell Technology Enabling Low-Power Operation and Stable Fabrication

— New memory cell structure employing Ta_2O_5 interfacial layer —

Tokyo, December 11, 2006— Hitachi, Ltd. (NYSE:HIT / TSE:6501) and Renesas Technology Corp. today announced the development of a new cell technology that will enable stable fabrication of phase-change memory while maintaining low-power operation performance.

The newly developed cell technology involves forming an interfacial layer of tantalum pent-oxide (Ta_2O_5) between the plug*[1] that connects to a MOS transistor and the phase-change film, and optimizing the thickness of the interfacial layer. In prototype phase-change memory cells fabricated using this structure, programming operation has been verified with a current of 100 µA at a power supply voltage of 1.5 V. In addition, the excellent adhesion between the Ta_2O_5 interfacial layer and phase-change film has the potential to provide enhanced stability in memory cell fabrication.

Phase-change memory, a type of nonvolatile memory that can be programmed and read, employs Joule heat generated by current and makes use of the difference in the electrical resistance of a film when in an amorphous state*[2] (high resistance) and when in a crystalline state (low resistance). The different electrical resistances represent the data values 1 and 0. Compared with conventional nonvolatile memory types, phase-change memory provides faster programming and read speeds, support for a higher number of rewrite cycles, and lower production cost. It is also well suited to integration, giving it great potential as a next-generation high-integration on-chip nonvolatile memory type.

In conventional phase-change memory it was necessary to heat the phase-change film material to past the melting point during resetting (amorphization). This required a large current of 1 mA or more. Then last year Hitachi and Renesas Technology developed a phase-change film made of oxygen-doped GeSbTe (germanium-antimony-tellurium), and succeeded in fabricating prototype memory cells with lower power requirements. These memory cells require a programming current of only 100 µA when using a power supply voltage of 1.5 V. However, the structure of the cell is such that it is easy for the heat generated in the phase-change film to escape via the plug. This causes the temperature rise during resets to be gradual and was thought to inhibit further reductions in the power requirements. In addition, GeSbTe, the material generally used for the phase-change film, exhibited poor adhesion with the silicon oxide film below it. This raised the need to deal with peeling problems in the phase-change memory fabrication process.

In their efforts to overcome this problem, Hitachi and Renesas Technology have developed a cell technology employing a new configuration. It achieves low-power operation and fabrication stability at the same time.

The newly developed technology uses a cell structure in which an ultrathin Ta_2O_5interfacial layer is formed between the phase-change film and the plug. This interfacial layer made of Ta_2O_5 prevents heat diffusion from the phase-change film via the plug. As a result, the temperature rise in the phase-change film is rapid, and the melting point is reached using less power.

In addition, the adhesion between the Ta_2O_5 interfacial layer and the phase-change film is excellent, increasing the peel strength of the film. Furthermore, by optimizing the method used to form the Ta_2O_5 layer, it is possible to reduce the resistance variation in a wafer. In this way the issue of GeSbTe peeling during the fabrication process is resolved, and the resistance variation is reduced. The result is greater stability in the memory cell fabrication process.

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The phase-change film used in the new memory cells is made of GeSbTe, which is the material in general use for this purpose. The prototype phase-change memory cells employing the new configuration have a verified programming current of 100 μA when using a power supply voltage of 1.5 V. In addition, the resistance variation in a wafer is limited, with a ratio in two digits between the high and low resistance values, and the ability to withstand 100million rewrites has been achieved.

The new technology will promote the realization of the next generation of high-integration on-chip nonvolatile memory and will be expected to lead to new advances in MCUs for embedded devices.

The results will be presented at the 2006 International Electron Devices Meeting to be held in San Francisco, U.S.A. from December 11.

<Terminology >

1. Plug: A piece of metal material that is embedded in an interlayer connecting hole (through hole).

2. Amorphous state: A state of matter in which the atoms and molecules that make up a solid are in an indeterminate arrangement that differs from the regular structure of a crystal. The term noncrystalline is also used to refer to this state.

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