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Prototype 2 Mbit Non-Volatile RAM Chip Employing Spin-Transfer Torque Writing Method

Leading the way for scalability of high-speed low power non-volatile RAM

Tokyo, 13th February 2007 --- Hitachi, Ltd. (NYSE: HIT / TSE: 6501) and the Research Institute of Electrical Communications (RIEC) of Tohoku University, have cooperated in the fabrication of a prototype of the world's first 2 megabit (Mbit) non-volatile random access memory (RAM) chip employing the spin-transfer torque writing method[*1]. A next-generation memory device, the Spin-transfer torque RAM (henceforth SPRAM), is receiving much attention as a strong candidate for a "universal memory," as it combines the advantage of various types of memory - the high speed characteristics of Static RAM (SRAM), scalability of Dynamic RAM (DRAM), and the non-volatility of FLASH memory - as well as low power requirements. This research result supports the advantage of SPRAM as a future universal memory, and opens the way to integrating the various types of memory currently being used in PCs, mobile equipment, etc., into one universal memory chip.

This work is part of a project (Project Leader: Prof. Hideo OHNO, RIEC) conducted with the support of the IT program of the Research Revolution 2002 (RR2002): Development of universal low-power spin memory, from the Ministry of Education, Culture, Sports, Science and Technology of Japan (MEXT).

In recent years, SPRAM has been attracting much attention as a "universal memory" - a next-generation memory, combining the best properties of various conventional memories (namely, excellent scalability characteristics and non-volatility enabling high-speed and low-power operation). SPRAM exploits the change in electrical resistance caused by a reversal in the direction of magnetization in the ferromagnetic film as a result of electron spin behavior when current is passed through a TMR[*2] device. As the current required for recording data can be reduced according to the scale of the device, SPRAM is considered a candidate for gigabit-class "universal memory". In contrast to conventional semiconductors, where the basic memory operation of a "1" or "0" signal is controlled by turning a current "on" and "off", with SPRAM, a specialized circuit operation, namely, changing the direction of current flowing in the TMR device depending on whether the signal is "1" or "0", is necessary. Further, measures need to be taken to prevent data from being written by a reading current (so-called "miswriting"). Thus, to realize a SPRAM chip mounted on peripheral circuits, it is necessary to bring together and combine, materials and device technology to achieve a high-performance TMR device, as well as advanced semiconductor circuit technology.

In response to this challenge, a collaborative research team set up by Hitachi and Tohoku University, undertook to develop new memory circuit technology using the spin-transfer torque writing method, by employing MgO[*3] which they had been independently developing, as the tunnel insulation film for a TMR device capable of low power write and high-output read operations. The prototype, a 2 Mbit SPRAM capable of high-speed operation (write time 100 nanoseconds (ns), read-out time 40 ns) at a low power of 1.8 V, was produced through a reciprocal collaboration process where Hitachi undertook the fabrication of the CMOS[*4], and RIEC undertook fabrication of the high-output TMR device at its Laboratory for Nanotechnology and Spintronics. Close cooperation made such an operation process possible, and has opened the way to the realization of a world-leading universal non-volatile memory.

1. Circuit technology for switching bi-directional current
   The signal-writing circuit in a conventional semiconductor memory is configured as a unidirectional circuit, where a current runs off from a bit line to ground via a memory cell. In contrast, current must flow bi-directionally in SPRAM; therefore, two bit lines are set up for one memory cell and depending on the direction of the current, one of the bit lines assumes the role of ground in response to the current direction. Further, a switch was incorporated in the circuit to change the direction of current flowing in the TMR device, and information is written by switching the direction of the writing current for each bit.

2. Circuit technology to prevent "miswriting" during reading
   In spin-transfer torque writing method, as current must flow in the TMR device during both read and write, there is a risk that information may be mistakenly rewritten by the read current. To understand this problem, the characteristics of a TMR device during read-out were analyzed, and it was found the occurrence of "miswriting" was related to the direction of read-current, and that the electrical resistance ratio of the TMR device required during read becomes larger as the bit-line voltage becomes lower. This finding was applied to overcome the "miswriting" issue by reducing the bit line voltage to a low 0.7V using the current flow from the top to bottom in the TMR device.

Operation of the prototype 2 Mbit SPRAM chip fabricated with 0.2 μm CMOS process was verified, and a high performance of 100 ns write and 40 ns read operation at a low voltage of 1.8 V was confirmed. Attaining a high sensitivity with a large electrical resistance ratio has made it possible to achieve high-speed readout at a low voltage. This result establishes fundamental circuit technology for SPRAM that is favorable towards scaling and low-power, and opens the way to achieving a gigabit-class universal memory.

These results were presented at the IEEE International Solid-State Circuits Conference (ISSCC 2007), held from 11th - 15th February 2007, in San Francisco, California, U.S.A.

■ Notes

*1 Spin-transfer torque writing method, also known as “spin-transfer switching” or “current-induced magnetization switching”

*2 TMR: Tunnel Magneto-Resistance

A tunnel magneto-resistance device is composed of a three layer structure of an insulating film sandwiched between ferromagnetic films. The change in current resistance which occurs when the magnetization direction of the upper and lower ferromagnetic layers change (parallel or anti parallel) is known as the TMR effect, and ratio of electrical resistance between the two states is known as the magnetoresistance ratio.

*3 MgO: Magnesium oxide.

In 2004, a research team at the National Institute of Advanced Industrial Science and Technology (AIST) successfully observed a magnetoresistance ratio of 180% in a room-temperature TMR device using pure iron as the ferromagnetic layers and magnesium oxide (MgO) as the insulating film. Following this, ANELVA Corporation reported a room-temperature TMR device with a magnetoresistance ratio of 230% using ferrocobalt boron as the ferromagnetic layer and MgO as the insulating film. In April 2005, the Hitachi-RIEC team observed the highest room-temperature magnetoresistance ratio of 287%, and further studies have lead to the achievement of a room-temperature magnetoresistance ratio of 450%. A TMR device using an aluminum oxide insulation film has a maximum magnetoresistance of approx. 70%.

*4 CMOS: Complimentary metal oxide semiconductor

About Hitachi, Ltd.

Hitachi, Ltd., (NYSE: HIT / TSE: 6501), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 356,000 employees worldwide. Fiscal 2005 (ended March 31, 2006) consolidated sales totaled 9,464 billion yen ($80.9 billion). The company offers a wide range of systems, products and services in market sectors including information systems, electronic devices, power and industrial systems, consumer products, materials and financial services. For more information on Hitachi, please visit the company's website at http://www.hitachi.com.

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