FOR IMMEDIATE RELEASE

Verification of 3.0 mW power consumption per 1 Gb/s in 100 Gb/s optical transmission with a prototype compact optical receiver for high-speed and low-power board-to-board signal transmission in IT equipment

- -Four-channel 25 Gb/s optical receiver mounted on a compact 16×16 mm package- -

Tokyo, Japan, September 24, 2010 – Hitachi, Ltd. (NYSE: HIT/TSE: 6501, hereafter, Hitachi) today announced the successful of development of a prototype compact optical receiver for 100 Gb/s[*1] transmission with a power consumption of 3.0 mW per 1 Gb/s - less than one-third the power required in conventional optical receivers, as part of its efforts to achieve board-to-board data transmission in IT equipment such as network equipment using a high-speed, low-power-consuming optical signals. This technology will be fundamental in achieving high performance but low power consuming next-generation IT equipment. The technology developed is the receiver section of the 100 Gb/s optical transceiver, a central component in the optical backplane signal-transmission[*2] technology currently being developed by Hitachi, and realizes a compact high-speed energy-efficient optical receiver. This work was supported in part by the “Next-generation High-efficiency Network Device Project,” contracted to the Photonics Electronics Technology Research Association (PETRA) by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

With the spread of the Internet, the information volume handled by network equipment is increasing year by year. According to the estimation given by the Ministry of Economy, Trade and Industry, Japan,[*3] if unattended, the power consumption in the year 2025 will be 13 times that of 2005. As 12% of power consumption in network equipment is due to board-to-board signal transmission in IT equipment, this represents 5% of total power consumption by IT equipment and is an enormous amount of electrical power. Conventionally, board-to-board signal transmission (namely, backplane signal transmission) in IT equipment such as network equipment uses parallel

electrical transmission technology. Currently, the transmission speed per channel is below 10 Gb/s in standard backplane signal transmission. As the transmission speed per channel increases beyond 20 Gb/s with future improvements in equipment processing power, increased signal-transmission loss[*4] due to increased power consumption will become obvious. To overcome this situation, the application of optical signal transmission with low transmission loss even at high speeds, to backplane transmission is being investigated. In order to switch to optical transmission, however, circuits to convert electrical signals into optical signals and vice versa, are required, and the increased power consumption by such circuits was an issue. To solve this issue, Hitachi is taking part in the NEDO project to develop a low-power-consumption compact optical transceiver for the achievement of optical backplane transmission.

The 100 Gb/s optical receiver developed co consists of four-channel 25 Gb/s optical receiver composed of a photodiode which converts optical signals into electrical signals and a trans-impedance amplifier which converts and amplifies electrical signals into voltage signals, mounted on a compact 16×16 mm package. In order to suppress crosstalk between adjacent channels, a shield mounting technique and a high-speed circuit scheme based on low-power CMOS process[*5] technology were also developed. The compact high-speed low-power optical receiver was achieved through the application of this technology.

The main features of the compact optical receiver developed are as described below.

(1) 25 Gb/s per channel four-channel mounting technique

A compact high-speed 100 Gb/s optical receiver is made possible by integrating four channels of 25 Gb/s per channel transmission signals and receiving them en bloc, however narrowing the width between the adjacent channels to decrease the size of the unit causes crosstalk between the wires (bonding wires) connecting the photodiode and the TIA, leading to degradation of signal quality. To overcome this, the photodiode and the TIA were mounted on a multi-layer ceramics package which effectively confines electromagnetic field, successfully reduced the crosstalk between adjacent wires using an electromagnetic shield

(inner-layer shield) set up between the circuit boards.

(2) Improvement of high-frequency characteristics to achieve 25 Gb/s

Using circuit-board wiring with an inner-layer shield to suppress crosstalk between adjacent wires, however, raises the problem of high-frequency signal transmission difficulties. In order to improve the high-frequency characteristics of the circuit-board wiring, a gain-control function which compensates only the high-frequency components of a signal was developed. Based on this function, a mechanism was established to enable signals including 25 Gb/s high frequency to be transmitted without interruption via the circuit-board wiring.

A prototype 25 Gb/s TIA chip was fabricated using the 65 nm CMOS process. When the power property was evaluated in comparison to a conventional TIA based on silicon-germanium bipolar transistors operating at high speed, the TIA developed operated at a power consumption of 3.0 mW which is less than one-third the power consumption per data rate. In addition, by suppressing the crosstalk between adjacent channels during 25 Gb/s operation to mount 25 Gb/s × four channels giving a total 100 Gb/s optical receiver on a 16×16 mm package, high-speed simultaneous reception was confirmed. The next step will be to integrate the optical transmitter which is being concurrently developed in the same package, to achieve an optical transceiver.

These results were presented at the IEEE Custom Integrated Circuits Conference which was held from 19th to 22nd September 2010 in San Jose, U.S.A. and at the European Conference and Exhibition on Optical Communication which was held from 19th to 23rd September 2010 in Turin, Italy.

Notes

*1. 100 Gbps: 1 gigabit equals 1 billion bits; 100 gigabits equals 100 billion bits.

*2. Backplane transmission: In large-scale IT equipment, data is transmitted via the backplane, a large printed-circuit board in the chassis of the equipment. By connecting many boards to the connectors on the backplane, data is transmitted between the boards (mounted with LSIs).

*3. Source: “The expectation for innovative energy-saving technology for information and communications equipment,” The Ministry of Economy, Trade and Industry, Japan,

October 2010, (in Japanese).

*4. Transmission loss: The degree of degradation of a signal being transmitted along a wire. Since transmission loss increases as data rate increases, the power consumption to compensate for the higher loss also increases.

*5. CMOS (complementary metal-oxide semiconductor) process: A silicon-based semiconductor-device structure that combines nMOS (negative MOS) transistors, which make free electrons the charge, and pMOS (positive MOS) transistors, which makes holes (i.e., parts of a solid crystal structure missing an electron) the charge. Since either of these transistors is always off, an electric current does not flow through the one that is off during operation, so the power consumption is very small.

About Hitachi, Ltd.

Hitachi, Ltd., (NYSE: HIT / TSE: 6501), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 360,000 employees worldwide. Fiscal 2009 (ended March 31, 2010) consolidated revenues totaled 8,968 billion yen ($96.4 billion). Hitachi will focus more than ever on the Social Innovation Business, which includes information and telecommunication systems, power systems, environmental, industrial and transportation systems, and social and urban systems, as well as the sophisticated materials and key devices that support them. For more information on Hitachi, please visit the company's website at http://www.hitachi.com.

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