Hitachi Releases SoC Emulator Incorporating SH2-DSP Core

— Allows SoC device verification before actual chip protoyping,
enabling system development time to be shortened —

Tokyo, September 20, 2001 — Hitachi, Ltd. (TSE: 6501) today announced the SoC Emulator as a development tool for custom SoCs (Systems on Chip) incorporating an SH2-DSP SuperH™*[1] RISC microcomputer core. Sales will begin in December 2001 in Japan.

This emulator incorporates an evaluation chip with an SH2-DSP core, and FPGAs (Field Programmable Gate Array) that enables writing of peripheral modules, user logic circuits, and so forth, making it possible to implement the same functions as an SoC device. This allows an SoC device to be verified while connected to the user system prior to actual chip protoyping, making it possible to shorten the user's system software and hardware development times.

At present, the main debugging tool for hardware such as a board and software such as a system program in developing a system that uses a microcomputer is an in-circuit emulator that allows verification by performing actual functional operations. Hitachi has previously released products including the E10, E20, and E8000 as emulators for the development of systems using standard SuperH microcomputer products. Meanwhile, for custom SoC devices incorporating peripheral modules, IP (Intellectual Property), user-designed logic circuits, and so forth, such as custom LSIs, verification has been carried out using software such as a simulator or logic emulator, with the resultant problems of slower operating speeds than the actual device and the inability to perform hardware debugging of peripheral functions. There has thus been a strong demand for an emulator capable of high-speed operation and actual functional operation while offering low cost and ease of use for the development of custom SoC devices.

The present SoC Emulator has been designed to meet this need. It comprises the following four types of board, and is used connected to a current E10A, E20, or E8000S emulator. The configuration and features of this new product are summarized below.

[Configuration]

(1) Evaluation chip board [165×220×20 (mm)]: Main board mounted with SH2-DSP core evaluation chip

(2) FPGA expansion board [100×145×10 (mm)]: Expansion board connecting FPGA board (3)

(3) FPGA board [165×185×20 (mm)]: Board mounted with FPGA for logic circuit writing

(4) Device control board for E8000S connection [141.8×254×20 (mm)]: Board for E8000S connection

[Features]

(1) Same functions as actual chip implemented by installation of FPGA board
One board is mounted with an FPGA enabling the configuration of two peripheral modules or 200K-gate circuitry, and a maximum of six boards can be connected. A SuperH microcomputer internal bus and external bus are connected to the FPGA, enabling peripheral modules and logic circuits incorporated in an SoC device to be configured with FPGAs, providing the same functions as an actual chip. In addition, functions that cannot be implemented with an FPGA, such as an analog interface, can be added to an FPGA board.

(2) Real-time tracing possible using maximum 80 MHz operating frequency
An SH2-DSP with a maximum operating frequency of 80 MHz is incorporated, enabling real-time operational verification of an SoC device. It is also possible to carry out hardware debugging of the internal circuits of an SoC device, verification of which has not previously been possible.

(3) Highly efficient software development by real-time operation
OS(Operating System) or the software running on OS, such as middleware or application software, is possible to operate by real-time operation. This reduces the software debugging time and makes the highly efficient software development.

(4) Choice of optimal combinations with current emulators according to the development level
This new product is used in combination with a current E10A, E20, or E8000S emulator, allowing the user to select the best combination--with the full-function E8000S, compact E20, or card-type E10A--to suit the development level and content. In addition, ease of use has been improved by such means as simplifying connection to the user system for greater compactness.

A Windows®*2 compatible PC can be used as the host computer. An ISA bus, PCI bus, PCMCIA bus, and LAN interface are provided as standard interfaces, and development of a USB interface is also planned for the future. Hitachi's comprehensive development environment HEW (Hitachi Embedded Workshop), linking various kinds of software including a C++ compiler, debugger, and linker, is provided as a user interface, enabling highly efficient development to be carried out.

Future plans include the development of products offering even greater ease of use, as well as products supporting other CPU cores.

Notes: 1. SuperH is a trademark of Hitachi, Ltd.
2. Windows is a registered trademark of Microsoft Corporation in the USA and other countries.

< Prices in Japan > (For Reference)

Product Code	Description	Price per Board (Yen)
HS0076EBK81H	Evaluation chip board	377,000
HS0076EFG81H	FPGA expansion board	377,000
HS0076EFPA1H	FPGA board	325,000
HS0076EDD81H	Device control board for E8000S connection	377,000

< Specifications >

Installed CPU core	SH2-DSP
Operating frequency	80MHz (max)
User logic (FPGA board)	• Per board: (1) 200K gates or (2) two peripheral modules (IP) • Expandable up to six boards
User I/F	Four 200-pin connectors