Hitachi Releases Industry's Smallest Analog Front-End ICs for CCD Cameras

— Offering smaller size together with low noise and low power consumption for use in digital cameras —

Tokyo, October 15, 2001 — Hitachi, Ltd. (TSE: 6501) today announced the HD49334 Series of CCD*[1] camera analog front-end ICs, offering high performance, low power consumption, and low cost, for use in digital cameras and similar products. Four models have been developed, including the HD49334NP/HNP in the industry's smallest QFN 36-pin package, and sample shipments will begin on October 16, 2001 in Japan.

A CCD camera analog front-end IC processes analog images from a CCD into digital signals that can be handled by a DSP or similar digital image signal processing IC, and is a key device in determining the performance of a CCD camera. With the major concern being the achievement of high performance together with low power consumption, this new series offers an approximately 3 dB S/N (Signal/Noise) improvement and approximately 20% lower power consumption than previous Hitachi products.

[Background]

The total number of digital cameras shipped worldwide in 2000 was 13 million, a 125% increase over the previous year, and the forecast for 2001 is 17 million units, an increase of 30% over 2000 (Hitachi figure). With this growth in the demand for CCD camera products, including digital still cameras and digital video cameras, there is fierce competition among set manufacturers to achieve higher functionality and performance at lower cost. Smaller size is another important requirement, and the features demanded of ICs to be installed in such products are high performance, low power consumption, and low cost, together with small size.

In response to these demands, Hitachi has employed its well-established and highly rated analog design technologies to develop the four models in the HD49334 Series.

A CCD camera analog front-end IC carries out the following kinds of processing on analog images picked up by a CCD, to produce digital signals.

(1) Noise elimination: The noise component in a signal output by the CCD is eliminated by a CDS circuit *[2].

(2) Signal amplification: A weak CCD output signal is adjusted to an optimal level by a PGA*[3] circuit.

(3) Conversion to digital signals: Analog signals are digitized by an ADC*[4] circuit in order to be supplied to a later-stage digital image signal processing IC.

[About these Products]

Major features of this new series are summarized below.

(1) Higher performance
The CDS circuit achieves high-precision suppression of low-band noise in signals received from the CCD, improving the S/N figure by approximately 3 dB compared with Hitachi's current HD49325 Series.
Also, there has long been a problem of the appearance of false colors with photographic subjects for which there is a gradual change in brightness. With this new series, a new approach has been applied to the CCD camera analog front-end IC output format, enabling an improvement of 6 dB or more (compared with previous Hitachi products) in the false color phenomenon.

(2) Lower power consumption
Optimization of the ADC circuitry and the power level of the amplifiers within the IC has resulted in an approximately 20% reduction in power consumption compared with Hitachi's current HD49325 Series.

(3) Lower Cost
Functional optimization has made it possible to improve performance while reducing the chip size, and so achieve lower cost.

(4) Smaller Size
In addition to the well-established QFP 48-pin ($9.0 \times 9.0 \times 1.7$ (mm)) package lineup, an ultra-small QFN 36-pin package ($6.2 \times 6.2 \times 0.9$ (mm))--an industry first for a CCD camera analog front-end IC--has been newly developed to meet the demand for smaller size. The QFN-36 package offers an approximately 53% reduction in package area and 75% reduction in cubic capacity compared with a QFP-48 package, enabling end-products to be made smaller.

This new series offers a variety of operating frequencies and packages to meet different user needs, with a lineup comprising the 25 MHz HD49334F (QFP-48 package) and HD49334NP (QFN-36 package), and the 40 MHz HD49334HF (QFP-48 package) and HD49334HNP (QFN-36 package).

Notes: 1. CCD: Charge coupled devices
2. CDS: Correlated double sampling
3. PGA: Programmable gain amplifier
4. ADC: Analog-to-digital converter

< Typical Applications >

Digital still camera, digital video cameras, monitoring cameras, etc.

< Prices in Japan > (For Reference)

Product Code	Operating Frequency	Package	Sample Price (Yen)
HD49334F	25MHz	QFP-48	360
HD49334NP		QFN-36	430
HD49334HF	40MHz	QFP-48	570
HD49334HNP		QFN-36	650

< Specifications >

Product Code	**HD49334F**	**HD49334NP**	**HD49334HF**	**HD49334HNP**
ADC precision	10 bits (1.5-bit pipeline)			
Differential/integral linearity	DNL : ±0.3LSB, INL : 2LSBp-p			
Power supply voltage	3 V ± 0.3 V			
Power consumption	66 mW typ. (25 MHz operation, 3.0 V)		130 mW typ. (40 MHz operation, 3.0 V)	
Operating frequency	25MHz		40MHz	
PGA gain control width	-2.36 dB to 31.40 dB / 8-bit control			
ADC input	ADC direct input supported			
Other items	(1) Approx. 3 dB S/N improvement compared with previous Hitachi products (2) 6 dB or more false color improvement through use of new ADC output format			
Packages	QFP-48	QFN-36	QFP-48	QFN-36