Development of 50-nm Gate-length CMOS Technology for Mobile Equipment

- Novel structure improves high-speed, low-power and high-frequency performance -

Tokyo Japan, December 5, 2001 - Hitachi, Ltd. (NYSE:HIT) has developed 50-nm gate length CMOS (Complementary Metal Oxide Semiconductor) device technology for high-speed, low-power, and high frequency applications, in the 0.1 μ m technology node. This technology achieves high-speed operation at low power; low noise performance for analog and RF applications using a novel Super Steep Channel structure, and high-speed using an Offset Source/Drain structure. It is expected to be suitable CMOS technology for the expanding mobile equipment market.

Advances in system LSIs performance have contributed largely to the rapid expansion of the market for mobile equipment, which are becoming increasingly functionally sophisticated in recent years. The performance of system LSIs for mobile equipment is characterized by operation speed and power consumption. For mobile communication equipment, analog and high frequency performance are also required. To reduce power consumption of CMOS devices in a system LSIs, one effective method is to reduce the operating voltage, however this also results in a reduction in operation speed. In addition, although high integration can be achieved at low cost with CMOS devices, a high noise level problem has prevented their widespread use in analog/RF applications until now. However, as further enhanced functionality of mobile equipment is predicted, the development of CMOS technology that provides low-power, high-speed, and low-noise performance in high-frequency regions, has become an urgent issue.

Hitachi undertook research in CMOS platform technology for the 0.1µm generation, and developed CMOS technology providing excellent low-voltage, high-speed and low noise performances.

Features of the technology are as follows:

(1) Super-Steep Channel (SSC): channel structure to improve low-power/RF performance. The SSC structure was developed to drastically reduce the impurity concentration in the channel region (the region through which current flows between the source and the drain) which obstructs high-speed operation, thus achieving high-speed operation at low voltage regions[*1)]. Further, this structure can prevent the formation of electrical defects that contribute to the noise of transistors[*2)].

(2) Offset Source/Drain Structure: transistor structure to achieve high-speed operation. The smaller the gate, which controls the on/off of a device, the higher is its speed. Therefore, an offset spacer was used to control the gate area, reducing gate capacitance. High-speed operation was achieved by this structure.

Using this technology, a prototype CMOS device with a gate length of 50nm was fabricated.

(more)

When compared with previous CMOS, an 8% increase in speed was achieved. It was also confirmed that a 6 dB [*3)] decrease in noise was possible. This result shows the improvement in basic CMOS performance using a 50nm gate-length CMOS. The next step will be to integrate the device into an LSI, and further develop CMOS platform technology for mobile equipment.

<Notes & Explanations of Terms>

(1) Features of low voltage and high-speed operation achieved using the heavy ion dopant profile: When a transistor is operated at the low-voltage, it is essential to increase the mobility of the carrier (electron and hole) to maintain operation speed. As carrier mobility decreases in a highly doped region, a channel region with low impurity concentrations needs to be formed. In this work, a super-steep dopant profile was achieved in the channel region by using a heavy ion that does not diffuse easily, thus achieving high-speed operation at low voltage.

(2) Decreasing the noise generation centers for noise reduction: Causes of the 1/f noise generation of transistors, are the trap levels [* 4)] around the gate insulator and the dopants in the channel region. With the super-steep channel technology, the punchthrough stopper ions are implanted in the channel region before gate insulator fabrication. As the trap levels generated in the gate insulator are reduced and channel dopant concentration is lower than with the conventional method , a decrease of 1/f noise becomes possible.

(3) A decrease of 6 dB (decibels); approximately 1/2 the noise level.

(4) Trap level: If ion implantation occurs through the gate dielectric, the chemical bonds around the gate insulator are broken, and become electrically unstable (trap level). The trap level is a cause of minute fluctuations in current as it captures and releases the carriers (electrons and holes which form the current flow in the channel) randomly.

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