Hitachi Releases SH7705 Ultra-Low-Power 32-Bit SuperH™ RISC Microprocessor

— Large 32-Kbyte cache memory and comprehensive on-chip peripheral functions including USB Function, enabling implementation of high-performance, low-power-consumption digital home appliances, portable information devices, and OA products—

Tokyo, July 22, 2002— Hitachi, Ltd. (TSE: 6501) today announced the SH7705 ultra-low-power microprocessor for use in digital home appliances such as digital still cameras and video printers, portable information devices such as electronic personal organizers and electronic dictionaries, and OA products such as fax machines and color printers. It incorporates an SH-3 32-bit CPU core of SuperH™*[1] RISC microprocessor family, large 32-Kbyte cache memory and a various kind of peripheral functions such as a USB (Universal Serial Bus) Function. Sample shipments will begin in August 2002 in Japan.

The SH7705 has an SH-3 SuperH family CPU core designed for low-power-consumption products, and is suitable for use in embedded systems that require high performance and low power consumption. A 0.18-um CMOS process is used, and ultra-low power consumption of 200 mW (typ.) at 133 MHz operation has been achieved. The SH7705 also incorporates large 32-Kbyte cache memory, four times the capacity of Hitachi's existing device, as well as a rich variety of on-chip peripheral functions including a USB Function, making possible end-products that offer lower power consumption, higher performance, and lower price.

Recently, In the fields of digital home appliances, portable information devices and OA products, end-products with a USB interface for connection to external devices are increasing, and Hitachi has previously released the SH7622, with an SH2-DSP CPU core and an on-chip USB Function, as a product designed for this market. However, with the larger data volumes and processing speeds associated with end-products that handle voice and image data, there is an ongoing trend toward even higher system performance and functionality. At the same time there is a demand for lower power consumption for such products as portable information devices, and a growing need for semiconductor devices that will meet these needs together with the requirement of lower end-product cost.

In response to these market demands, Hitachi is releasing the SH7705 32-bit RISC microprocessor that offers higher performance though the use of an SH-3 CPU core, a upper model than the SH2-DSP, together with even lower power consumption than existing device. Features of the SH7705 are summarized below.

< Product Features >

1. Ultra-low power consumption of 200 mW (typ.) at 133 MHz operation
   The SH7705 employs a 0.18-um CMOS process and dual power supply voltages of 1.5 V and 3.3 V. By operating internal logic circuit at a low voltage of 1.5 V, power consumption of 200 mW (typ.) at 133 MHz operation has achieved and has become ultra-low power consumption approximately half that of the current SH7622 in power consumption per processing performance unit (W/MIPS). In addition, a module standby function that halts unnecessary modules offers a further order of reduction in power consumption, enabling longer battery-driven operation time of portable information products.

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2. High performance achieved by incorporation of SH-3 CPU core and large 32-Kbyte cache memory
   The SH7705 incorporates a high-performance SH-3 CPU core designed for portable devices, enabling processing performance of 173 MIPS at 133 MHz operation. It is an approximately 30% improvement over the 130 MIPS at 100 MHz operation of the SH7622 incorporating an SH2-DSP core. In addition, cache memory capacity has been quadrupled, and cache memory can be accessed internally in one clock cycle, for higher processing speed.

3. On-chip USB Function, enabling high-speed data exchange with a PC, etc., plus comprehensive peripheral functions
   The SH7705 incorporates a USB Function supporting USB Standard Ver. 1.1. Control, interrupt, and bulk transfers are supported, with a fast data transfer capability of maximum 12 Mbps (bits per second). A USB transceiver is also incorporated, enabling the number of parts to be reduced. A variety of other peripheral functions are also provided, including high-speed serial interfaces with a 64-byte FIFO (First In First Out), MMU (Memory Management Unit) and DMAC, interfaces for various kinds of memory such as synchronous DRAM, and an IrDA (Infrared Data Association) Ver. 1.0 interface for infrared communication. This enables lower-cost of high-performance products.

Two packages are available: a 208-pin LQFP (28 mm × 28 mm) and a 208-pin CSP (12 mm × 12 mm). On-chip debugging functions (H-UDI and AUD) are incorporated, enabling real-time emulation to be carried out at the maximum operating frequency using an E10A PC card emulator. In addition, SolutionEngine®*2 for the SH7705 is available as an application development platform, facilitating speedy and efficient software development.

Hitachi plans to further enhance its lineup of products for use in digital home appliances, portable information devices, and OA products, and to develop products offering significantly higher performance and lower power consumption.

Notes: 1. SuperH is a trademark of Hitachi, Ltd.
2. SolutionEngine is a registered trademark in Japan of Hitachi ULSI Systems Co., Ltd.

< Typical Applications >

- Digital home appliances such as digital still cameras and digital video camera
- Portable information devices such as electronic personal organizers and electronic dictionaries
- OA products such as digital still camera printers and fax machines

< Prices in Japan >(For Reference)

Product Code		Operating Frequency	Package	Sample Price (Yen)
SH7705	HD6417705F133	133 MHz	LQFP-208	1,700
	HD6417705F100	100 MHz	LQFP-208	1,600
	HD6417705BP133	133 MHz	CSP-208	1,800
	HD6417705BP100	100 MHz	CSP-208	1,700

< **Specifications** >

Item		**SH7705**	
Product code		HD6417705F133	HD6417705F100
		HD6417705BP133	HD6417705BP100
Power supply voltage		Internal: 1.4 V to 1.6 V, external: 3.0 V to 3.6 V	
Operating frequency		133 MHz	100 MHz
Processing performance		173 MIPS	130 MIPS
CPU core		SH-3	
Cache memory configuration		32 Kbytes (mixed instructions/data, 4-way set-associative, write-through/write-back selectable, LRU method)	
MMU		128-entry, 4-way set-associative TLB	
On-chip peripheral functions and interfaces		• DMAC × 4 channels • USB Function (USB Standard Ver. 1.1 supported) • 32-bit timer × 3 channels • 16-bit timer pulse unit × 4 channels • Real-time clock • A/D converter × 4 channels • IrDA Ver. 1.0 • Serial interface × 2 channels (built-in transmit/receive 64-byte FIFO, synchronous/asynchronous mode)	
Bus state controller		• Flash memory with page mode function/SRAM/synchronous DRAM interface • Supports up to 8 address space areas	
Power-down modes		• Four modes: Sleep mode, software standby mode, hardware standby mode, module standby mode	
power consumption		200 mW (typ. at 133 MHz operation)	
Debugging functions		• On-chip debugging functions (H-UDI, AUD)	
Packages	HD6417705F133 HD6417705F100	• 208-pin LQFP (28 mm × 28 mm, 0.5 mm pin pitch)	
	HD6417705BP133 HD6417705BP100	• 208-pin CSP (12 mm × 12 mm, 0.65 mm pin pitch)	

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.
