Hitachi Develops H8SX 32-bit CPU Core for High-Speed, High-Performance CISC Microcomputers, and Releases H8SX/1650 for PC Peripherals and OA Devices as H8SX First Product

— CPU core offering software compatibility with current Hitachi 16-bit microcomputers plus approximately tripled performance for high-performance systems —

Tokyo, January 16, 2003— Hitachi, Ltd. (TSE: 6501) today announced the development of the 32-bit H8SX, using Hitachi's original architecture, as a CPU core for CISC (Complex Instruction Set Computer) microcomputers. The first product to be released incorporating this CPU core is the H8SX/1650, for use in PC peripherals such as optical storage devices and in OA and consumer products. Sample shipments will begin in April 2003 in Japan.

A CISC microcomputer is equipped with a complex instruction set including a large number of instructions such as bit control and other instructions. Although it is generally difficult to achieve the high operating frequencies of RISC (Reduced Instruction Set Computer) microcomputers, CISC microcomputers have certain advantages such as ease of programming which have led to their use in a variety of products. Hitachi has previously released the 8-bit H8/300 Series and 16-bit H8/300H Series, higher speed version H8S series that meet a variety of user needs. However, with the increasing speed and performance of PC peripherals, OA devices, and consumer products, there is a strong demand for higher-performance CISC microcomputers.

To meet this market need, Hitachi has developed the H8SX CPU core based on 16-bit H8S CPU core, with the bus width extended to 32 bits. The H8SX CPU core is designed for use in a wide range of application areas, including PC peripherals, OA and consumer products, and automotive equipment. The evaluation chip has shown an increase in maximum operating frequency from the 33 MHz of current Hitachi 16-bit microcomputers to 48 MHz, and achieved an approximately threefold increase in performance over previous models. A variety of peripheral functions are also provided. Products incorporating this CPU core have also been developed as the H8SX Series. The first model to be released in this series is the H8SX/1650 (35MHz operating frequency), designed for use in PC peripherals such as optical storage devices and in OA and consumer products.

Features of the H8SX CPU core and the H8SX/1650 are summarized below.

< H8SX CPU Core Features >

1. Achieving an approximately threefold increase in processing power over previous Hitachi models

The H8SX CPU core employs a 0.18 micron CMOS process, and achieves a maximum operating frequency of 48 MHz, an approximately 50% improvement over the 33 MHz of current 16-bit microcomputers. This, together with doubling of the bus width to 32 bits, has resulted in an approximately threefold improvement in processing power. Multiplier performance has been improved and a divider has been incorporated, enabling high processing performance of 48 MIPS (Dhrystone 1.1) to be attained. To simplify connectivity to peripheral devices, the H8SX CPU core includes a function for conversion to little-endian format and an address/data multiplex bus I/O interface that can be set for each area of external memory, enabling fewer external parts to be used than with previous products, while also reducing the software load.

2. Improved code efficiency with addition of new instructions

   The instruction set of the H8SX CPU core features upward-compatibility with current 16-bit microcomputers plus the addition of new instructions and addressing modes. This allows programs written for current microcomputers to be used, while enabling higher system performance to be achieved through improved code efficiency and extension of the bus width to 32 bits. In addition, expansion of the address space enables the size of programs and data to be increased in line with higher system functionality.

3. Preparation of enhanced peripheral functions for sophisticated systems

   A variety of peripheral functions designed for products with future expandability are provided on an evaluation chip, providing for smooth lineup product development. In addition to enhanced versions of the peripheral functions incorporated in current 16-bit microcomputers, the H8SX CPU core includes new functions not present in 16-bit models. Peripheral functions include data transfer modules such as a DTC (Data Transfer Controller), DMAC (Direct Memory Access Controller), and EXDMAC (External DMAC) that provide highly efficient internal and external data transfer, and a serial communication interface with FIFO that prevent data transfer congestion and I2C bus interface. Also provided is a Multifunction Timer Unit (MTU) that simplifies the control of various kinds of motors, including stepping and DC brushless motors. The provision of these various interfaces on the evaluation chip will enable rapid development of H8SX Series products for sophisticated systems.

< H8SX/1650 Features >

1. Excellent cost-performance, for higher-performance, lower-cost systems

   A model with a 35 MHz maximum operating frequency, offering an excellent balance between cost and performance, is available for use in applications such as optical storage devices that demand high system speed and performance together with low cost. With processing performance more than double that of previous models, this will help users create high-performance products at lower cost.

2. Suitable for a wide range of applications, including PC peripherals and OA devices

   In addition to such basic peripheral functions as timers and serial interfaces, the H8SX/1650 includes eight 10-bit resolution A/D converter channels and two 8-bit resolution D/A converter channels. A little-endian conversion function and address/data multiplex I/O interface, not provided in current models, enable the H8SX/1650 to be used in a wide range of applications such as PC peripherals and OA products, as well as optical storage devices.

The E6000H full emulator is under preparation as a development tool.

Future plans for the H8SX Series provide for extension of the product lineup to include a high-speed version and models with on-chip flash memory, as well as a USB (Universal Serial Bus) and other peripheral functions, and the development of ASSP models for use in consumer, automotive, and other application areas.

Note: Company and product names mentioned in this Press Release are trademarks or registered trademarks of the respective companies.

< Typical Applications >

- PC peripherals such as optical storage devices (CD-R/RW, DVD-R/RW, DVD-ROM/RAM, etc.)
- OA devices and consumer products

< Price in Japan >(For Reference)

Product Code	Package	Sample Price (Yen)
H8SX/1650 (HD6411650)	TQFP-120	900

< **Specifications** >

Item	**H8SX/1650 (HD6411650)**	**Note: Evaluation chip**
CPU core	32-bit H8SX core	
Maximum operating frequency	35 MHz	48 MHz
Power supply voltage	3.0 V to 3.6 V	3.0 V to 3.6 V
On-chip RAM	24 Kbytes	64 Kbytes
External Address space	16 Mbytes	16 Mbytes, 256 Mbytes
External bus width	8/16 bits	8/16/32 bits
Calculation Units	On-chip multiplier, divider, multiply-and-accumulate processor	
Bus state controller	ROM, SRAM, burst ROM, byte-control SRAM directly connectable	ROM, SRAM, DRAM, synchronous DRAM, burst ROM, byte-control SRAM directly connectable
	Address/data multiplex I/O interface settable area by area	
	Endian conversion function for connection of little-endian devices	
On-chip peripheral functions	—	DMA controller (DMAC) × 4 channels
	—	EXDMA controller (EXDMAC) × 4 channels
	Data transfer controller (DTC)	Data transfer controller (DTC)
	Timer pulse unit (TPU) × 6 channels	Timer pulse unit (TPU) × 12 channels
	Programmable pulse generator (PPG)	
	—	Multifunction timer unit (MTU) × 5 channels
	8-bit timer (MTR) × 4 channels	8-bit timer (MTR) × 8 channels
	Watchdog timer (WDT) × 1 channel	Watchdog timer (WDT) × 1 channel
	—	Advanced user debugger (AUD)
	—	Hitachi user debug interface (H-UDI)
	Serial communication interface × 4 channels	Serial communication interface × 6 channels
	—	Serial communication interface with FIFO × 1 channel
	—	I^2C bus interface × 2 channels
	A/D converter (10-bit resolution) × 8 channels	A/D converter (10-bit resolution) × 16 channels
	D/A converter (8-bit resolution) × 2 channels	D/A converter (8-bit resolution) × 6 channels
	Clock pulse generator (CPG): Built-in multiplication PLL	Clock pulse generator (CPG): Built-in multiplication PLL

Power-down modes	Sleep mode	
	Software standby mode	
	Hardware standby mode	
	Module stop mode	
	All modules clock stop mode	
	Multi clock mode	
Package	TQFP-120	BGA-600

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.
