10th February 2003
Hitachi, Ltd.

Prototype SRAM for mobile equipment achieves world's lowest standby current

- Prevention of cosmic ray-induced soft error leading to significant increase in reliability -

Hitachi, Ltd. (NYSE:HIT) has developed circuit technology for SRAM (Static Random Access Memory), used in cellular phones and personal digital equipment, which has achieved the world's lowest standby leakage current (16.7 femto-ampere (FA)/cell; femto: one quadrillionth, 10^{-15}) and reduced cosmic ray-induced soft-error*1) rate to one two-hundreth ($^{1}/_{200}$) of previous levels. The technology developed is circuit technology which not only significantly reduces power consumption during standby, but also solves the problem of cosmic ray-induced soft error which arises as a result of increasing device miniturization.

SRAM is currently used as memory in cellular phones and personal digital equipment, due to its low power consumption features. However, as design-scales decrease in the pursuit greater SRAM memory capacity, several problems arise. Firstly, as the thickness of the gate insulation layer, of which the device is composed, becomes extremely thin at several nanometers (nm; 10^{-9}m) or less, the leak current (the tunnel current between the gate and the silicon substrate) increases dramatically, causing power consumption during standby, i.e. when the SRAM is not operating, to increase. Another problem, is the appearance of the hitherto insignificant at ground-level problem of cosmic ray-induced soft error phenomenon. In the past, there was a period when soft error caused by alpha rays*2) was a problem for DRAM (Dynamic Random Access Memory). However, as the mechanism of the soft error caused by cosmic rays and alpha rays differ, it was not possible to apply the same error correction technology. Such problems were expected to become even more prominent with design rules beyond the 130nm-process which is already being used, and thus development of new technology to overcome them was an urgent matter.

In response to the need for new technology to overcome problems arising from increased miniaturization of SRAM devices, Hitachi has developed two new circuit technologies. Details of the technology are as follows.

(1) **Electric-field-relaxed (EFR) circuit technology to reduce gate leakage current:** Gate leak current occurs where there is a strong electric field. Therefore circuit technology which reduces the electric fields in the transistor by optimizing the supply voltage applied to each of the 4 signal and power lines (word line, bit line, power line,

earth line) of each memory cell (the minimum unit of memory) was developed. This is the first time in the world that a reduction in tunnel leakage current has been achieved by circuit design.

(2) **Alternate error checking and correction circuit technology for high accuracy correction of cosmic ray-induced soft:** The Production Engineering Research Laboratory of Hitachi, Ltd. (henceforth PERL; GM: Dr. Katsuki MIYAUCHI) analyzed the effect of cosmic rays on semiconductor devices, and discovered a characteristic pattern in the position of memory cells which were destroyed by cosmic rays. By using the pattern characteristic, and allocating a different address to the memory cells susceptible to destruction, circuit technology which enabled high accuracy error checking and correction of the destroyed memory cell was developed.

When a 16 megabit SRAM prototype was made using these circuit technologies with a 130nm CMOS process, gate leakage current was decreased by 90%, and cosmic ray-induced soft error rate was reduced to one two-hundreth of previous levels. The standby current attained per cell was 16.7 fA/cell, the lowest in the world.

This technology can be applied not only to independent SRAM memory but also cache memory (on-chip memory) integrated in system LSIs, and is expected to be indispensable circuit technology for the 130nm process generation and beyond.

This technology was announced at the International Solid-State Circuits Conference (ISSCC), which was held from 9th February 2003, in San Francisco, California, U.S.A.

►Explanation of Terms

(1) Cosmic ray-induced soft-error: Cosmic-rays penetrate silicon, and generate electric charges. These electric charges are collected in the storage node, and affect the data.

(2) Alpha-ray soft error: Alpha rays are the flow of helium (He) nuclei generated by radioactive impurity. Alpha rays penetrate silicon, and generate electric charges. These electric charges are collected in the storage node of a cell, and affect the data. In past semiconductor memory, most of the soft error was caused by the alpha ray.

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